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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/769,510	01/30/2004	Michael Eneboe	01-490/1C	8371

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LSI CORPORATION
1621 BARBER LANE
MS: D-106
MILPITAS, CA 95035

EXAMINER	
SIEK, VUTHE	

ART UNIT	PAPER NUMBER
2825	

MAIL DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/769,510	ENEBOE ET AL.	
	Examiner	Art Unit	
	Vuthe Siek	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 July 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5,7-12 and 21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,7-12 and 21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to application 10/769,510 and amendment filed on 6/22/2007. Claims 1-5, 7-12 and 21 remain pending in the application.

Claim Objections

2. Claims 4, 11 and 21 are objected to because of the following informalities: the recitation of the claim is not proper format of Markush type claims (See MPEP 803.02). Appropriate correction is required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-5, 7-12 and 21 are rejected under 35 U.S.C. 103(a) as being obvious over Kastenholz et al. (5,980,543 B1) in view of Riley (6,871,248 B2) or Gulick et al. (6,148,357) or James et al. (6,414,971 B1).

5. As to claim 1 and 10, Kastenholz et al. teach an interconnect network for operation within communication node, wherein the interconnect network may have feature including the ability to transfer a variety of communication protocols, scalability bandwidth (bandwidth scalable interconnect network) and reduced down-time (optimized IC design). The interconnect network includes at least one local interconnect module (Fig. 2, interconnect modules) having local transfer elements for transferring information between a plurality of I/O channels and scaling elements for expanding the

interconnect network to include additional local interconnect modules, such that information can be transferred between the local interconnect modules included in the interconnect network (Fig. 3). The local interconnect modules include substantially the same integrated circuit as claimed (ASICs or self-programmable integrated circuit) (Fig. 3, 5, 8 and 11). The processor 1114 includes a CPU module, DRAM, FPGA control and Ethernet control, much in the same way that memory 710, controller 712 and control and status registers 753 provide these functions for local interconnect board. The invention efficiently attains the objects set forth in the disclosure, including providing dynamically bandwidth scalable interconnect network (col. 24 lines 7-15, see summary). One advantage of the invention is that the communication node can process information entering the node at a variety of speeds and formatted pursuant to a plurality of protocols (optimized heuristic data) (col. 7 lines 13-54). Kastenholz et al. do not the integrated circuit is optimized based on isochronous interconnect configuration. Numerous patents recited an optimal isochronous interconnect configuration for used in a computer system (communications field) so that an entire path of the computer system guarantees a quality of service level corresponding to the required bandwidth and with service windows within the minimum and maximum service windows of the original request for an isochrounous channel (interconnect) and also to ensure isochronous transactions can proceed without being blocked by non-isochronous traffic (col. 10 lines 18-39, summary of Riley). Gulick et al. teach isochronous interconnect of used communications field for transferring isochronous data (summary). James et al. teach an interconnect transmission line is configured to transmit isochronous data

packets in communications field (summary; col. 6 lines 46-62). It would have been obvious to practitioners in the art at the time the invention was made to have optimized the IC as taught by Kastenholz et al. based on isochronous interconnect configuration because the optimized IC including all interconnect capacities, scalability of the interconnect channel capacities and isochronous interconnect configuration would expect that an entire path of the computer system (IC) to guarantee a quality of service level corresponding to the required bandwidth and with service windows within the minimum and maximum service windows of the original request for an isochrounous channel (interconnect) and also ensure isochronous transactions can proceed without being blocked by non-isochronous traffic (col. 10 lines 18-39, summary of Riley).

6. As to claims 2-5, 7-9,11-12 and 21, Kastenholz et al. teach communication nodes including ASICs (self-programmable IC) including arrangement of components (Fig. 3, 5, 8 and 11). The processor 1114 includes a CPU module, DRAM, FPGA control and Ethernet control, much in the same way that memory 710, controller 712 and control and status registers 753 provide these functions for local interconnect board. The invention efficiently attains the objects set forth in the disclosure, including providing dynamically bandwidth scalable interconnect network (col. 24 lines 7-15, see summary). One advantage of the invention is that the communication node can process information entering the node at a variety of speeds and formatted pursuant to a plurality of protocols. The invention is also dynamic bandwidth scalability (operated without intervention by an agent (col. 7 lines 13-54)

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vuthe Siek whose telephone number is (571) 272-1906.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on (571) 272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Vuthe Siek/
Vuthe Siek
Primary Examiner, A.U. 2825